15. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces, at least one of the planar perimeter side surfaces extending [between] from the first planar surface [and] to the second planar surface, the entire at least one perimeter side surface having a ground or polished surface[;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape].

22. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more [planar] perimeter sides [side surfaces, at least one of the planar perimeter side surfaces extending between the first planar surface and the second planar surface];

[a layer of scribe material forming the planar perimeter side surfaces, the layer of scribe material surrounding the circuitry]; and

[means for treating the at least one planar perimeter side surface of the semiconductor die to provide the at least one planar perimeter side surface with a ground or polished surface] at least one of the perimeter sides having at least two offset planar surfaces that are substantially parallel to each other and ground or polished to remove irregularities from each of the two offset planar surfaces.

23. (Twice Amended) The semiconductor die as recited in claim 22, wherein each of the two offset [entire] planar [perimeter side] surfaces [extends between] is transverse to the first planar surface and the second planar surface [and is a ground or polished surface].

24. (Twice Amended) The semiconductor die as recited in claim 22, wherein [the] at least one of the two offset planar surfaces [planar perimeter side surface is transverse to] extends from at least one of the first planar surface and the second planar surface.

25. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [side surfaces] sides extending between the first planar surface and the second planar surface;

each perimeter side [surface] having offset perimeter planar surfaces, where the offset perimeter planar surfaces are substantially parallel to each other with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface, and each of the offset perimeter planar surfaces is a ground or polished surface[;

a layer of scribe material forming the perimeter side surfaces, the layer of scribe material surrounding the circuitry; and

the semiconductor die has an overall rectangular footprint].

35. (Twice Amended) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter [side surfaces] sides extending between the first planar surface and the second planar surface; and

at least one perimeter side [surface] having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface [, where the planar perimeter surfaces are substantially transverse to the first planar surface and the second planar surface].

41. (Thrice Amended) A semiconductor die comprising:

a first planar surface;

a second planar surface opposite the first planar surface;

one or more perimeter edges transverse to and extending between the first planar surface and the second planar surface; and

at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface; and

each offset planar surface having a ground or polished surface.

43. (Amended) The semiconductor die as recited in claim 41, wherein [the] each perimeter edge includes offset planar surfaces that are substantially parallel to one another, each of the offset planar surfaces on each perimeter edge are substantially transverse to the first planar surface and the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on October 18, 2002, and the references cited therewith. Claims 11, 15, 22-25, 35, 41 and 43 are amended and claim 40 is canceled; as a result, claims 11-25, 35-39 and 41-43 are now pending in this application.

Examiner Interview

Applicant's attorney would like to thank Examiner Pert for his courtesy during the telephone interview held on January 3, 2003. Examiner Pert and Applicant's attorney discussed the scope of the Ormond reference.